Introduction to Digital Logic Design Lab

EECS 31L

Lab 6

3/5/2020

1, Objective

In this lab, I intended to continue to design the single cycle processor.

2, Procedure

The design of this lab can, as the pervious lab, can be divided to 2 parts, which are the design of single component and the connection between components.

A, controller:

The controller has one input(opcode) and 6 outputs (aluop, regwrite, alusrc, memread, memwrite and mem2reg). The design is pretty straight forward because the only thing I did was to decide every single according the input using IF block.

B, ALU controller

The design of the ALU controller is quite straight forward too. As what I did in the design of the controller, the only thing I needed to do was to decide the output (Operation) according those 3 inputs (ALUOp, funct3 and funct7).

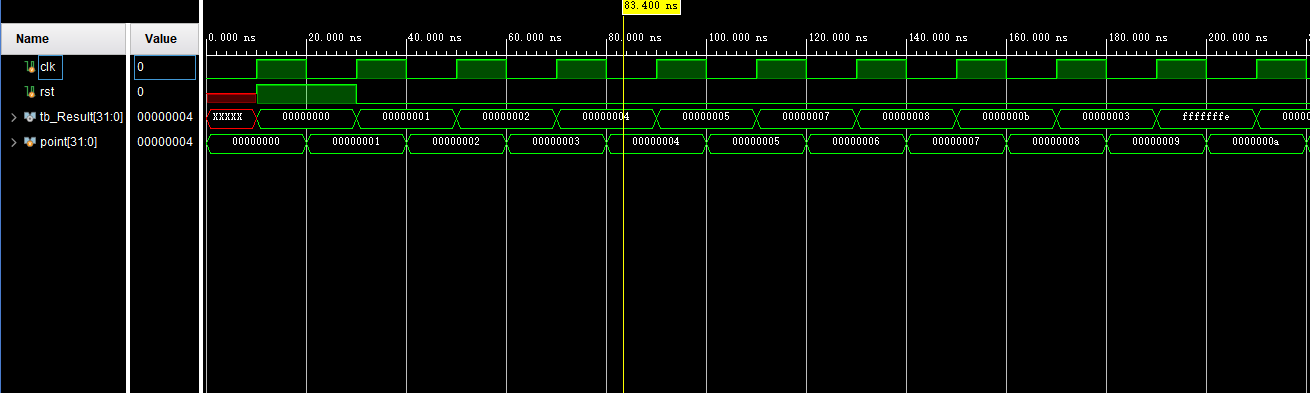
C, datapath

I already designed the datapath in the previous lab.

D, processor

The only thing I did was to connect every component together by defining wires that connects each component.

3, Simulation Results



Continued……….